CLAIMS

What is claimed is:

1. A system for generating sample locations that span a plurality of local coordinate systems, the system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit is configured to:

receive a two-dimensional bin address specifying a position of a bin in a local sample space region served by the circuit, and a two-dimensional bin offset of an origin of a coordinate system for the local sample space region with respect to an origin of a global sample space coordinate system that contains the local sample space region; and

generate an output sequence of one or more sample displacements that correspond to a pre-selected transformation applied to a pre-selected set of sample displacements corresponding to a global address, wherein the global address is the vector sum of the two-dimensional bin address and the two-dimensional bin offset.

2. The system of claim 1, wherein the pre-selected transformation is a pre-selected set of two or more transformations sequentially applied to a pre-selected set of sample displacements corresponding to the global address.

3. The system of claim 1, further comprising a plurality of graphics accelerators, wherein each graphics accelerator has one or more local coordinate systems L_K for a region R_K of global sample space, wherein each graphics accelerator comprises one or more rendering pipelines, sample buffers and filtering units, and wherein each rendering pipeline and each filtering unit has a sample generation circuit.

4. The system of claim 3, wherein each graphics accelerator generates video pixels corresponding to one or more regions of global sample space, and the plurality of

graphics accelerators collaboratively generate a composite image for one or more display devices.

5. The system of claim 3, wherein a host computer is operable to coordinate the generation of sample locations across the multiple local coordinate systems, by sending a two-dimensional offset for each local coordinate system L_K to the corresponding graphics accelerator.

6. The system claim 3, wherein a host computer is operable to send a two-dimensional composite offset to a first filtering unit in a first of said graphics accelerators, wherein the two-dimensional composite offset is a sum of (a) a displacement from an origin of the global sample space coordinate system to an origin of a first local coordinate system corresponding to the first graphics accelerator and (b) a displacement from an origin of the first local coordinate system to an origin of a sublocal coordinate system corresponding to the first filtering unit.

7. A system for generating sample locations that span a plurality of local coordinate systems, the system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit is configured to:

receive a two-dimensional bin address specifying a position of a bin in a local coordinate system corresponding to the circuit, and a two-dimensional bin offset of an origin of the local coordinate system with respect to an origin of a global sample space coordinate system;

determine a global address of the bin by forming the vector sum of the two-dimensional bin address and the two-dimensional bin offset; and

generate an output sequence of one or more sample displacements that correspond to a pre-selected transformation applied to a pre-selected set of sample displacements corresponding to the global address.

8. The system of claim 7, wherein the sample generation circuits reside in respective rendering units of a graphics accelerator, wherein a host computer is operable to set the two-dimensional bin offset of each sample generation circuit equal to a displacement from an origin of the global sample space coordinate system to an origin of a region served by the graphics accelerator.

9. The system of claim 7, wherein the sample generation circuits reside in respective filtering units of a graphics accelerator, wherein a host computer is operable to set the two-dimensional bin offset for each filtering unit is equal to a composite offset, wherein the composite offset equals a sum of (a) a displacement from an origin of the global sample space coordinate system to an origin of a region served by the graphics accelerator and (b) a displacement from an origin of the served region to an origin of a subregion corresponding to the filtering unit.

10. A system for generating sample locations that span a plurality of local coordinate systems, the system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit S_K is configured to:

receive a two-dimensional bin address specifying a position of a bin in a local sample space coordinate system L_K for the sample generation circuit S_K, and a two-dimensional bin offset of an origin of the local sample space coordinate system L_K with respect to an origin of a global sample space coordinate system:

add the two-dimensional local bin address and the two-dimensional bin offset to generate a two-dimensional global bin address;

select a first portion of the two-dimensional global bin address and identify a corresponding transformation based on the first portion and a pre-selected pattern of transformations that span global sample space;

apply an inverse of the identified transformation to a second portion of the two-dimensional global bin address, thereby generating a memory address for a sample bin containing pre-selected sample displacements;

read a first sequence of one or more sample displacements from the sample bin; and

generate an output sequence of sample displacements by applying the first transformation to the first sequence of sample displacements.

11. A system for generating sample locations that span a plurality of local coordinate systems, the system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit S_K comprises:

an adder unit configured to:

receive a two-dimensional bin address specifying a position of a bin in a local sample space coordinate system L_K for the sample generation circuit S_K, and a two-dimensional bin offset of an origin of the local sample space coordinate system L_K with respect to an origin of a global sample space coordinate system; and

add the two-dimensional local bin address and the two-dimensional bin offset to generate a two-dimensional global bin address;

a transformation control unit configured to receive a first portion of the two-dimensional global bin address and identify a corresponding transformation based on the first portion and a pre-selected pattern of transformations that span global sample space;

an address transform unit, wherein the address transform unit is configured to apply an inverse of the identified transformation to a second portion of the two-dimensional global bin address, thereby generating a memory address defining a bin from a tile of bins containing pre-selected sample displacements;

a sample location memory configured to store the pre-selected sample displacements for a tile of bins, wherein the sample location memory is configured to output a first sequence of sample displacements in response to receiving the memory address; and

an output transform unit, wherein the output transform unit is configured to apply the identified transformation to the first sequence of sample displacements in response to receiving the transformation code, thereby generating a second output sequence of sample displacements.

12. The system of claim 11, wherein the adder unit comprises an "x" component adder and a "y" component adder.

13. The system of claim 11, wherein the first portion of the global address is [Eb, Fb] and the second portion of the global address is [Ea, Fa]; wherein the horizontal component E of the two-dimensional global bin address is represented as E=[Ec,Eb,Ea]; wherein Ea is a contiguous set of least significant bits in E, Eb is a contiguous set of medium significant bits in E, and Ec is a contiguous set of next more significant bits in E; wherein sizes of Ea, Eb and Ec are "a" bits, "b" bits and "c" bits respectively; wherein the vertical component F of the two-dimensional global bin address is represented as F=[Fc,Fb,Fa], wherein Fa is a contiguous set of least significant bits in F, Fb is a contiguous set of medium significance bits in F, and Fc is a contiguous set of next more significant bits in F; and wherein sizes of Fa, Fb and Fc are "a" bits, "b" bits and "c" bits respectively, "a" and "b" are integers greater than or equal to one, and c is an integer greater than or equal to zero.

14. The system of claim 11, wherein the tile of bins containing pre-selected sample displacements is a rectangular array of sample bins.

15. A method for generating sample locations spanning a plurality of local coordinate systems, the method comprising:

receiving a two-dimensional bin address specifying a position of a bin in a local sample space region, and a two-dimensional bin offset of an origin of a coordinate system for the local sample space region with respect to an origin of a global sample space coordinate system that contains the local sample space region; and

generating an output sequence of one or more sample displacements that correspond to a pre-selected transformation applied to a pre-selected set of sample displacements corresponding to a global address, wherein the global address is the vector sum of the two-dimensional bin address and the two-dimensional bin offset.

16. The method of claim 15, wherein the pre-selected transformation is a pre-selected set of two or more transformations sequentially applied to a pre-selected set of sample displacements corresponding to the global address.

17. A method for generating sample locations that span a plurality of local coordinate systems, the method comprising:

receiving a two-dimensional bin address specifying a position of a bin in a local sample space region served by the circuit, and a two-dimensional bin offset of an origin of a coordinate system for the local sample space region with respect to an origin of a global sample space coordinate system that contains the local sample space region;

determining a global address of the bin by forming the vector sum of the two-dimensional bin address and the two-dimensional bin offset; and

generating an output sequence of one or more sample displacements that correspond to a pre-selected transformation applied to a pre-selected set of sample displacements corresponding to the global address.

18. A method for generating sample locations spanning a plurality of local coordinate systems, the method comprising:

transferring a plurality of two-dimensional bin offsets to a plurality of sample generation circuits respectively, wherein the two-dimensional bin offset transferred to each sample generation circuit S_K of the plurality of sample generation circuits equals the displacement of an origin of a corresponding local coordinate system L_K with respect to an origin of a global coordinate system, wherein each sample generation circuit S_K performs the actions of:

receiving a two-dimensional local address of a sample bin with respect to the local coordinate system L_K;

adding the two-dimensional local address to the corresponding two-dimensional bin offset to determine a two-dimensional global bin address;

operating on a first portion of the two-dimensional global bin address to identify a corresponding transformation based on the first portion and a pre-selected pattern of transformations that span global sample space;

applying an inverse of the first transformation to a second portion of the two-dimensional global bin address to determine a modified two-dimensional address;

reading first sample displacements from a sample location memory using the modified two-dimensional address; and

applying the first transformation to the first sample displacements to determine second sample displacements.

19. The method of claim 18, wherein each sample generation circuit S_K performs the additional action of adding the second sample displacements to the two-dimensional local address of the sample bin to generate local sample locations.

20. The method of claim 18; wherein the first portion of the global address is [Eb, Fb] and the second portion of the global address is [Ea, Fa]; wherein the horizontal component E of the two-dimensional global bin address is represented as E=[Ec,Eb,Ea]; wherein Ea is a contiguous set of least significant bits in E, Eb is a contiguous set of medium significant bits in E, and Ec is a contiguous set of next more significant bits in E; wherein sizes of Ea, Eb and Ec are "a" bits, "b" bits and "c" bits respectively; wherein the vertical component F of the two-dimensional global bin address is represented as F=[Fc,Fb,Fa], wherein Fa is a contiguous set of least significant bits in F, Fb is a contiguous set of medium significance bits in F, and Fc is a contiguous set of next more significant bits in F; and wherein sizes of Fa, Fb and Fc are "a" bits, "b" bits and "c" bits respectively, "a" and "b" are integers greater than or equal to one, and c is an integer greater than or equal to zero.

21. A method for selecting sample positions for a specific sample bin in a region of sample space corresponding to one of a set of clustered graphics accelerators comprising:

selecting sample locations for an Mi x Ni array of sample bins located in region(i) sample space by:

selecting sample locations for each sample bin of an n x n array of sample bins, wherein each bin has k sample locations, wherein $n=2^a$, and wherein a and k are positive integers;

storing the sample locations for the n x n array of sample bins in a memory;

selecting an m x m array of 2-D transformations;

applying the transformation specified at each position in the m x m array to the n x n array of sample bins to populate sample locations in an nm x nm array of sample bins, wherein $m=2^b$;

tiling the nm x nm sample bin array across the available sample space;

generating sample locations by using a logic circuit configured to:

sum the respectively x value and y value for sample bin location (x,y) in region(i) sample space coordinates and the x value and y value of bin (0,0) in region(i) in a global sample space coordinate system that spans the regions (i);

operate on the b+a least significant bits of the x and y sums to select a specific transformation T from the m x m array of transformations and to select a specific sample bin, from the n x n array of sample bins, that correspond to the sample bin location (x,y) in region(i); and

generate one or more sample positions by applying transformation T to a first one or more of the k sample positions stored in the memory for the specific sample bin.

22. The method of claim 21, wherein transformation T is a pre-selected set of two or more transformations that are sequentially applied.

23. A system for generating sample locations that span a plurality of local coordinate systems, the system comprising:

means for receiving a two-dimensional bin address specifying a position of a bin in a local sample space region served by the circuit, and a two-dimensional bin offset of an origin of a coordinate system for the local sample space region with respect to an origin of a global sample space coordinate system that contains the local sample space region; and

means for generating an output sequence of one or more sample displacements that correspond to a pre-selected transformation applied to a pre-selected set of sample displacements corresponding to a global address, wherein the global address is the vector sum of the two-dimensional bin address and the two-dimensional bin offset.

24. The system of claim 23, wherein the pre-selected transformation is a pre-selected set of two or more transformations sequentially applied to a pre-selected set of sample displacements corresponding to the global address.

25. A system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit is configured to:

receive a two-dimensional bin address specifying a position of a bin in a local coordinate system corresponding to the circuit, and a two-dimensional bin displacement of an origin of the local coordinate system with respect to an origin of a window;

determine a window-relative bin address of the bin by computing a vector sum of the two-dimensional bin address and the two-dimensional bin displacement;

generate an output sequence of one or more sample displacements that correspond to a transformation designated by the window-relative bin address.

26. The system of claim 25, wherein the sample generation circuits reside in respective rendering units of a graphics accelerator, wherein a host computer is operable to set the two-dimensional bin displacement of each sample generation circuit equal to a

displacement from an origin of the global sample space coordinate system to an origin of a region served by the graphics accelerator.

27. A system comprising:

a plurality of sample generation circuits, wherein each sample generation circuit S_K comprises:

an adder unit configured to:

receive a two-dimensional bin address specifying a position of a bin in a local sample space coordinate system L_K for the sample generation circuit S_K, and a two-dimensional bin offset of an origin of the local sample space coordinate system L_K with respect to an origin of a window; and

add the two-dimensional local bin address and the two-dimensional bin offset to generate a two-dimensional window-relative bin address;

a transformation control unit configured to receive a first portion of the two-dimensional window-relative bin address and identify a corresponding transformation based on the first portion and a pre-selected pattern of transformations;

an address transform unit, wherein the address transform unit is configured to apply an inverse of the identified transformation to a second portion of the two-dimensional window-relative bin address, thereby generating a memory address defining a bin from a tile of bins containing pre-selected sample displacements;

a sample location memory configured to store the pre-selected sample displacements for a tile of bins, wherein the sample location memory is configured to output a first sequence of sample displacements in response to receiving the memory address; and

an output transform unit, wherein the output transform unit is configured to apply the identified transformation to the first sequence of sample displacements, thereby generating a second output sequence of sample displacements.

28. The system of claim 27, wherein a host computer is operable to:

compute the two-dimensional bin offset for sample generation circuit S_K by subtracting (a) a displacement of the window with respect to an origin of a global sample space coordinate system from (b) a displacement of the local sample space coordinate system L_K with respect to the origin of the global sample space coordinate system; and

supply the two-dimensional bin offset to the sample generation circuit S_K;

repeat said computing and said supplying for each said sample generation circuits.

29. A system comprising:

a window ID table configured to output a displacement (W_X,W_Y) of a window with respect to an origin of a global sample space coordinate system in response to receiving a window ID;

a first register configured to store a displacement (N_X,N_Y) of a first coordinate system with respect to an origin of the global sample space coordinate system;

a sample generation circuit including:

a subtraction unit configured to compute a displacement (M_X,M_Y) by subtracting the displacement (W_X,W_Y) from the displacement (N_X,N_Y);

an adder unit configured to receive a bin address (X,Y) specifying a position of a bin in the first coordinate system, and to compute a window-relative bin address by adding the bin address (X,Y) to the displacement (M_X,M_Y);

a transformation control unit configured to receive a first portion of the window-relative bin address and identify a corresponding transformation based on the first portion and a pre-selected pattern of transformations;

an address transform unit, wherein the address transform unit is configured to apply an inverse of the identified transformation to a second portion of the two-dimensional window-relative bin address, thereby generating a memory address defining a bin from a tile of bins containing pre-selected sample displacements;

a sample location memory configured to store the pre-selected sample displacements for a tile of bins, wherein the sample location memory is

configured to output a first sequence of sample displacements in response to receiving the memory address; and

an output transform unit, wherein the output transform unit is configured to apply the identified transformation to the first sequence of sample displacements, thereby generating a second output sequence of sample displacements.

30. The system of claim 29, wherein a host computer is operable to:
compute and store the displacement (N_X,N_Y) in the first register;
store the displacement (W_X,W_Y) for each window of a collection of windows in the window ID table.

31. The system of claim 30, wherein the host computer is operable to:
update the displacement (N_X,N_Y) in response to a user movement of the window.

32. The system of claim 29, wherein the window ID is a component of a received sample accessed from a sample buffer.